CLAIMS

We Claim:

1. A fieldless array comprising:

a semiconductor region having a first conductivity type;

a plurality of oxide-nitride-oxide (ONO) structures formed over the upper surface of the semiconductor region;

a plurality of word lines formed over the ONO structures, wherein each of the ONO structures is substantially covered by one of the word lines.

2. The fieldless array of Claim 1, wherein the word lines comprise polycrystalline silicon.

3. The fieldless array of Claim 1, further comprising: a plurality of diffusion bit lines formed in the semiconductor region, wherein the diffusion bit lines have a second conductivity type, opposite the first conductivity type.

4. The fieldless array of Claim 3, further comprising: bit line oxide regions formed over the diffusion bit lines, wherein the word lines extend over the bit line oxide regions.

5. The fieldless array of Claim 1, further comprising dielectric sidewall spacers located adjacent to the word lines.

6. The fieldless array of Claim 1, further comprising gap-filling oxide located between the word lines.

7. A method of fabricating a fieldless array, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a surface of a semiconductor region;

patterning the ONO layer to create a first set of ONO structures that define locations for a plurality of diffusion bit lines of the fieldless array;

forming a plurality of word lines over the first set of ONO structures; and

patterning the first set of ONO structures, thereby creating a second set of ONO structures, wherein the second set of ONO structures are located entirely under the plurality of word lines.

8. The method of Claim 7, further comprising forming dielectric sidewall spacers adjacent to the word lines.

9. The method of Claim 7, further comprising forming gap-filling oxide between the word lines.

10. The method of Claim 7, further comprising implanting diffusion bit lines through the first set of ONO structures.

11. The method of Claim 10, further comprising thermally growing bit line oxide regions over the diffusion bit lines.

12. The method of Claim 10, wherein the diffusion bit lines extend along a first axis, and the word lines extend along a second axis, perpendicular to the first axis.

13. The method of Claim 10, wherein the steps of forming a plurality of word lines and patterning the first set of ONO structures comprise:

depositing a layer of polysilicon over the first set of ONO structures;

forming a photoresist mask over the layer of polysilicon;

etching the layer of polysilicon through the photoresist mask; and

etching the first set of ONO structures through the photoresist mask

14. The method of Claim 13, wherein the steps of etching the layer of polysilicon and the first set of ONO structures are implemented by a reactive ion etch (RIE).

15. The method of Claim 13, wherein the step of etching the first set of ONO structures is implemented by a series of wet etches.

16. The method of Claim 13, wherein the step of etching the first set of ONO structures is implemented by a wet etch and a dry/reactive ion etch (RIE).

17. The method of Claim 13, wherein the step of etching the first set of ONO structures is extended to etch the semiconductor substrate to a depth of 50 to 400 Angstroms.

18. The method of Claim 13, further comprising:

depositing a thin dielectric spacer having a thickness up to about 400 Angstroms over the etched layer of polysilicon; and then

etching back the thin dielectric spacer layer, prior to etching the first set of ONO structures.

19. The method of Claim 13, further comprising performing a re-oxidation step after the step of etching the first set of ONO structures.

20. The method of Claim 19, wherein the re-oxidation step results in the formation of about 20-200 Angstroms of silicon oxide.

21. The method of Claim 13, wherein the step of etching the first set of ONO structures results in the removal of portions of the ONO structure under the layer of polysilicon.